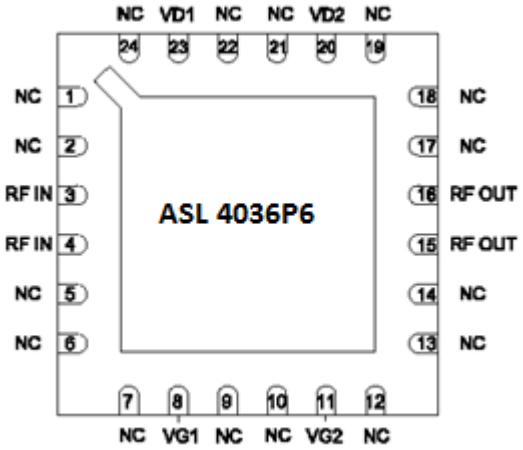
8.5 – 10.5 GHz 1 Watt Power Amplifier

Features

- Frequency Range : 8.5 – 10.5 GHz
- >29.5dBm output P1dB
- 14.5 dB Power gain
- 33% PAE
- High IP3
- Input Return Loss > 12 dB
- Output Return Loss > 8 dB
- Dual bias operation
- No external matching required
- DC decoupled input and output
- 0.5 µm InGaAs pHEMT Technology
- Open cavity QFN Package



Typical Applications

- RADAR
- Military & space
- LMDS, VSAT

Description

The ASL4036P6 is a X-band Power amplifier with 29.5 dBm output P1dB. The PA uses two stages of amplification and operates in 8.5 – 10.5 GHz frequency range. The PA features 14.5 dB of gain with input and output return loss of 12 dB and 8 dB respectively. The PA has a high IP3 of 38dBm and 33% PAE. This feature enables it to be used in the applications requiring efficiency along with linearity. The chip operates with dual bias supply voltage.The die is fabricated using a reliable 0.5µm InGaAs pHEMT technology.

The package used is a SMD open cavity QFN Package with base metal made up of copper composite.

Absolute Maximum Ratings (1)

Parameter	Absolute Maximum	Units
Drain bias voltage ($V_d = V_{d1} = V_{d2}$)	+9	volts
Total Drain current ($I_{dq1}+I_{dq2}$)	0.5	A
RF input power (RFin at V_d = 8V)	26	dBm
Operating temperature	-50 to +85	^oC
Storage Temperature	-65 to +150	^oC

1. Operation beyond these limits may cause permanent damage to the component

Electrical Specifications (1) @ T_A = 25 ^oC, T_B = 50 ^oC, $V_{d1} = V_{d2}$ = 8V, $V_{g1} = V_{g2}$ = -1V, Z_o =50 Ω

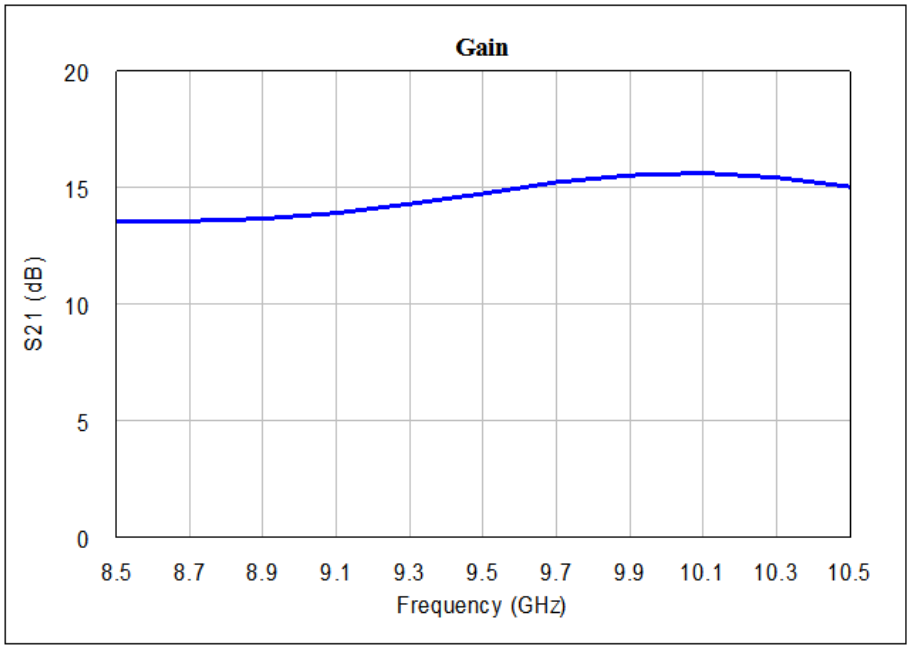
Parameter	Min.	Typ.	Max.	Units
Frequency Range		8.5 - 10.5		GHz
Gain	13.5	14.5		dB
Gain Flatness		+/-0.7		dB
Output Power (P1 dB)	29	29.5		dBm
Input Return Loss	8	12		dB
Output Return Loss	6	8		dB
Saturated output power (Psat)	29.5	30.5		dBm
Output Third Order Intercept (IP3)		38		dBm
Power Added Efficiency (PAE)		33%		--
Saturated Gain		11		dB
Gate Voltage ($V_g = V_{g1} = V_{g2}$)	-1.2	-1	-0.8	V
Supply Current (I_{dq})		330		mA
Supply Current (I_{dsat})		460		mA

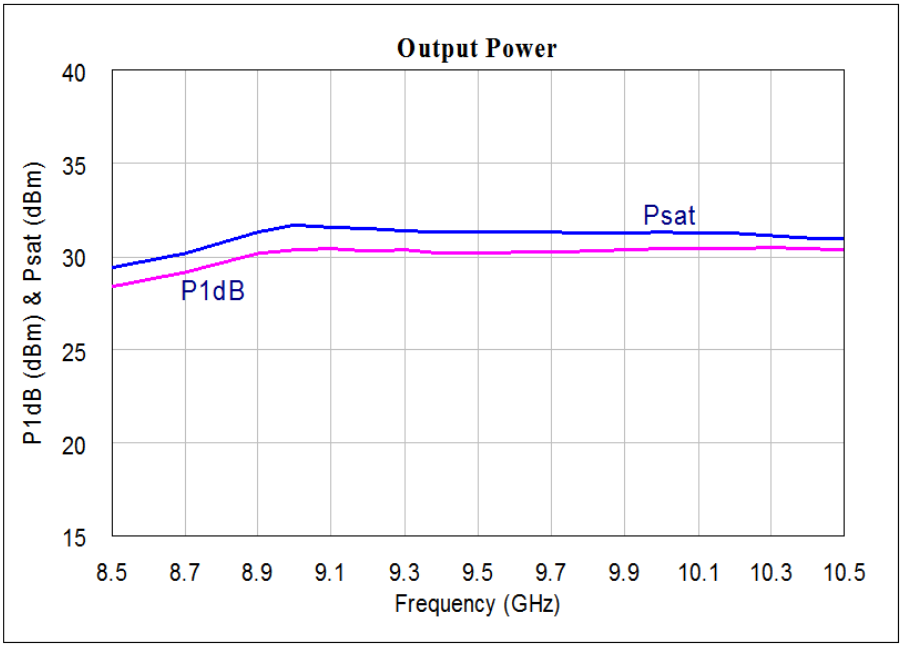
Note:

1. Electrical specifications as measured in test fixture.
2. T_A – Ambient Temperature; T_B – Base Plate Temperature
3. I_{dsat} - Drain Current at Saturated Output Power

Test fixture data

V_{d1} = V_{d2} = 8V, V_{g1} = V_{g2} = -1V, Total Current (I_{dq}) = 330mA, T_A = 25 ^oC





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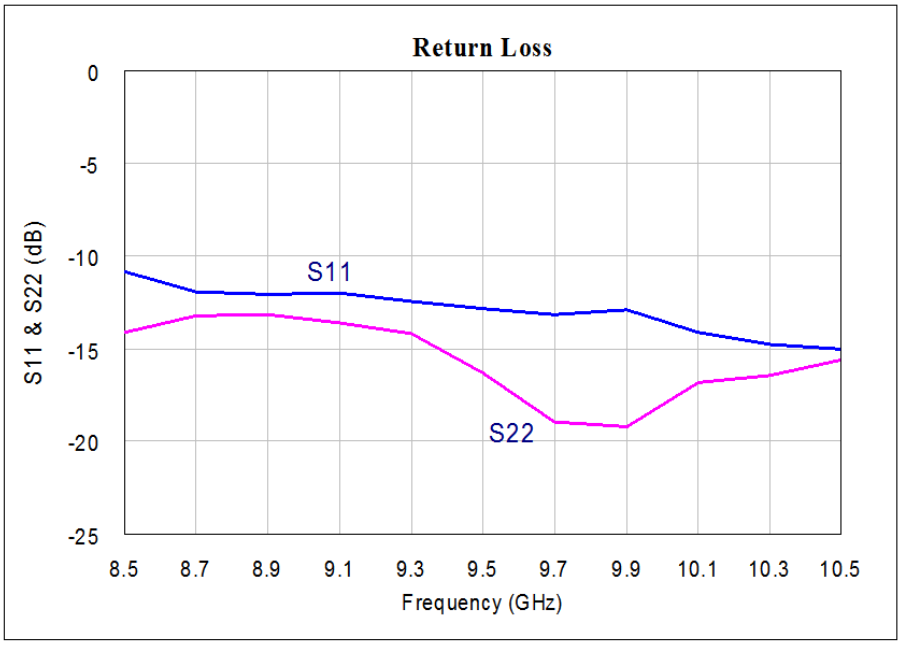
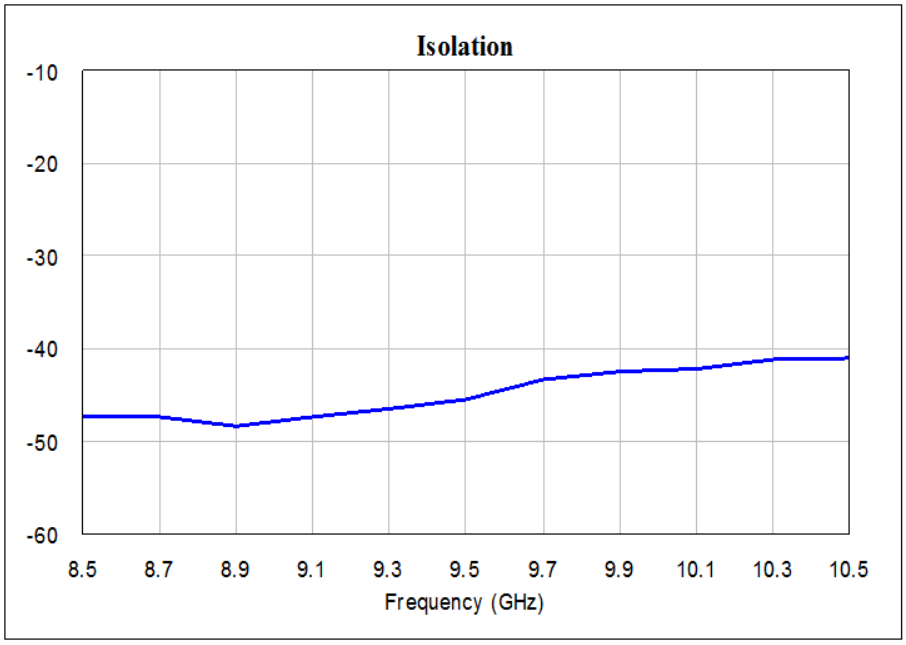
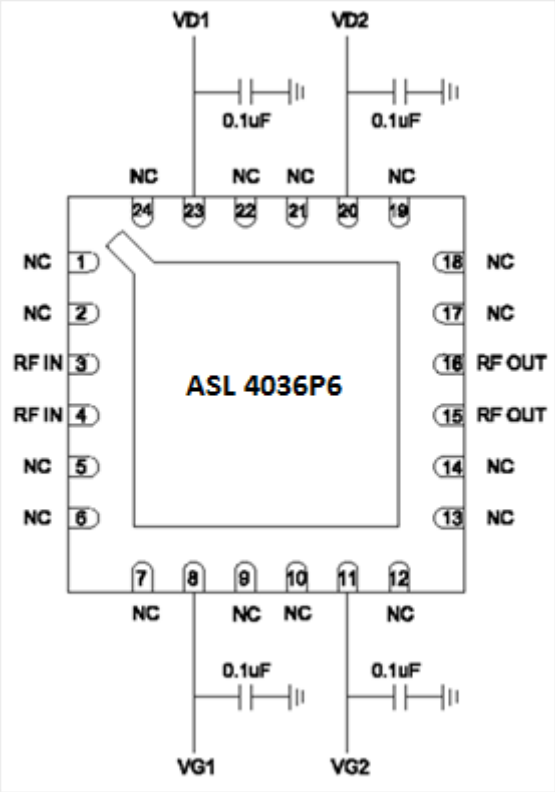




Pin details



Top View

Note:

1. All RF and DC bond pads are 100µm x 100µm
2. Pad no. 3,4 : RF IN
3. Pad no. 8,11 : Vg1, Vg2
4. Pad no. 23,20 : Vd1, Vd2
5. Pad no. 15,16 : RF OUT
6. Pad no. 1,2,5,6,7
   9,10,12,13,14,17
   18,19,21,22,24 : NC (No Connection)

Recommended Assembly Diagram

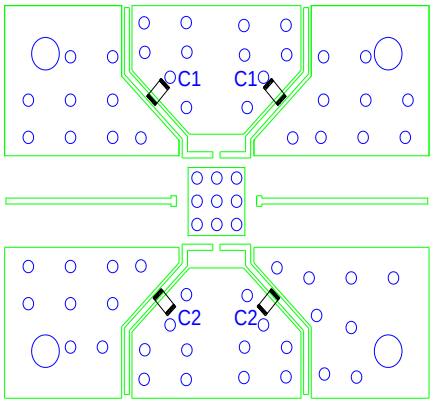


Fig: PCB Drawing

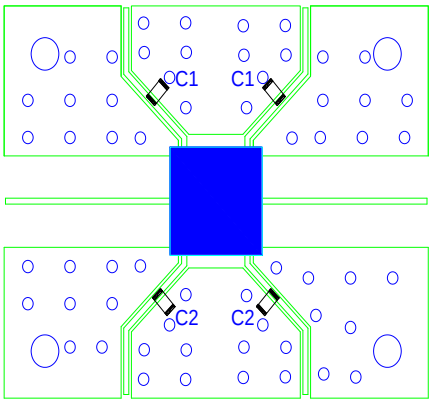
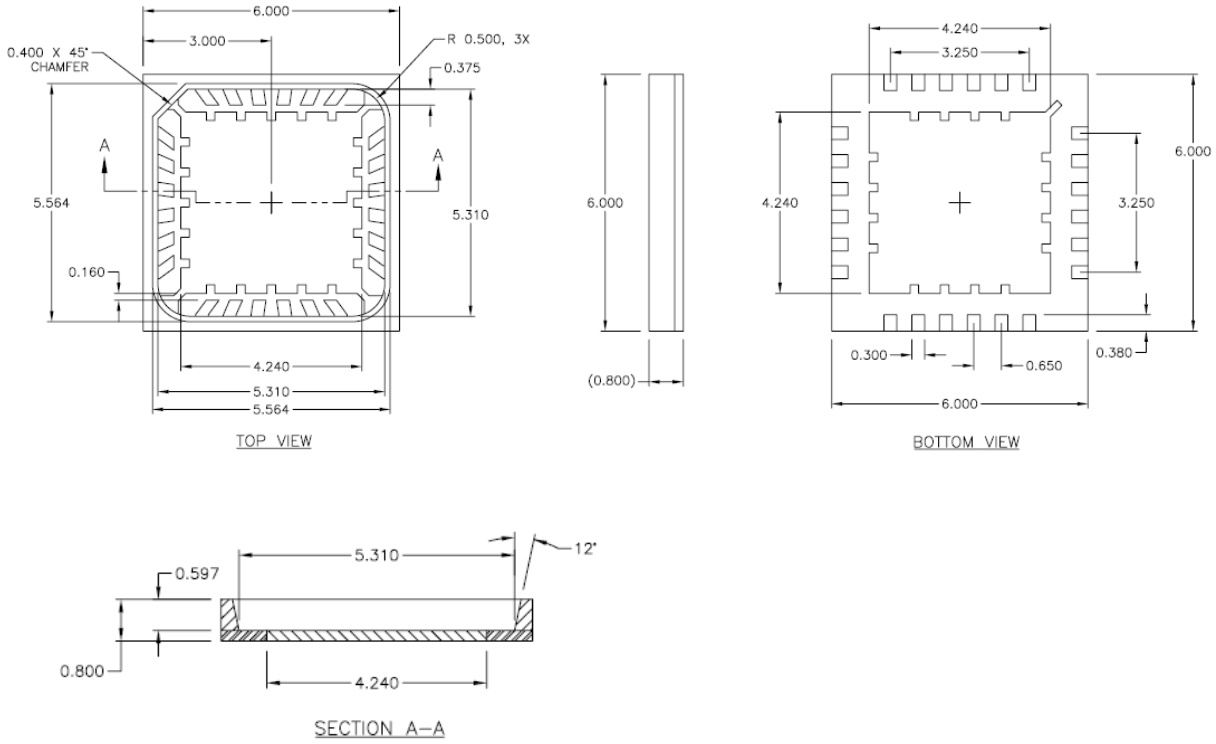


Fig: Package assembled on PCB

Note:

1. Input and output 50 ohm lines are preferably on 5 mil RT Duroid substrate.
2. C1 and C2 refers to 0.1uF multilayer chip bypass capacitors for drain and gate supplies.
3. 1µF capacitors may be additionally used as a second level of bypass at drain supply voltages for reliable operation.
4. The RF input & output ports are DC decoupled on-chip.
5. Proper heat sink like Alluminium or copper to be used for better reliability of package.

Package outline drawing



GaAs MMIC devices are susceptible to Electrostatic discharge. Proper precautions should be observed during handling, assembly & testing

All Information and Specifications are subject to change without prior notice. Before using the product, please refer to the latest datasheet available in the website.